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S-BAND SOLID STATE TRANSMITTER.(U)
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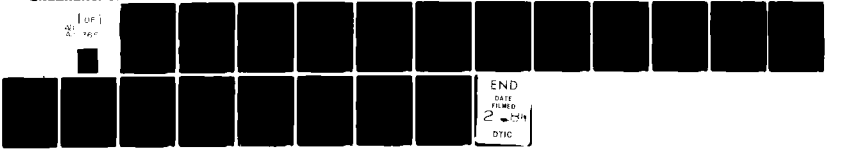

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LEVEL II

S-BAND SOLID STATE TRANSMITTER

February 1980

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Under Contract

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U.S. Army Material Development
and Readiness Command
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CONTENTS

FIGURES

1.0 INTRODUCTION

Solid-state power generation techniques are presently available which allow for the generation of high peak power in the S-band frequency domain. Transmitters so configured would have inherent advantages of ruggedness, improved reliability, simpler modulation, and total use of low voltage supplies which would make it an excellent replacement for thermionic transmitters presently used.

2.0 APPROACH

2.1 General

Given the objective of developing a solid state transmitter at high S-band and analyzing the availability of high power transistors presently available, the decision was made to generate the power at ½ fo and use a frequency doubler to achieve 80 watts peak in each of two channels.

A negative resistance transistor oscillator was chosen as the signal source followed by 4 stages of class C transistor amplification to attain the signal level of approximatley 190 watts at the input to the multiplier.

The 100nsec pulsewidth was accomplished by a packaged single-pole-single throw RF switch module and associated driver module.

The overall size of the unit is 6.4" x 5.1" x 1". Best use of the space was to construct a center septum as the ground plane with dielectric material and etched microstrip circuitry on both sides. Soft substrate materials[1] were chosen for the dielectrics. One side was low K (ε_r = 2.2) and the other was higher K (ε_r = 10.3), so that components could be fitted to the optimum material, figures 1 and 2.[2]

2.2 Evaluation of High Power Transistors

State-of-the-art transistors were available for evaluation from Power Hybrids, Incorporated (PHI) and from Microwave Semiconductor Corporation (MSC).

PHI devices were selected because they demonstrated about 75 watts at fo/2 for 14 watts of drive, as opposed to about 65 watts from the MSC parts. Table I is a data summary of ten of these devices.

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[1] Woermbke, James D., "Better Your MIC Designs with High -K Substrates, "Microwaves, Mar. 1979, pp. 66-68

[2] See Appendix A for complete listing of drawings available from HDL.

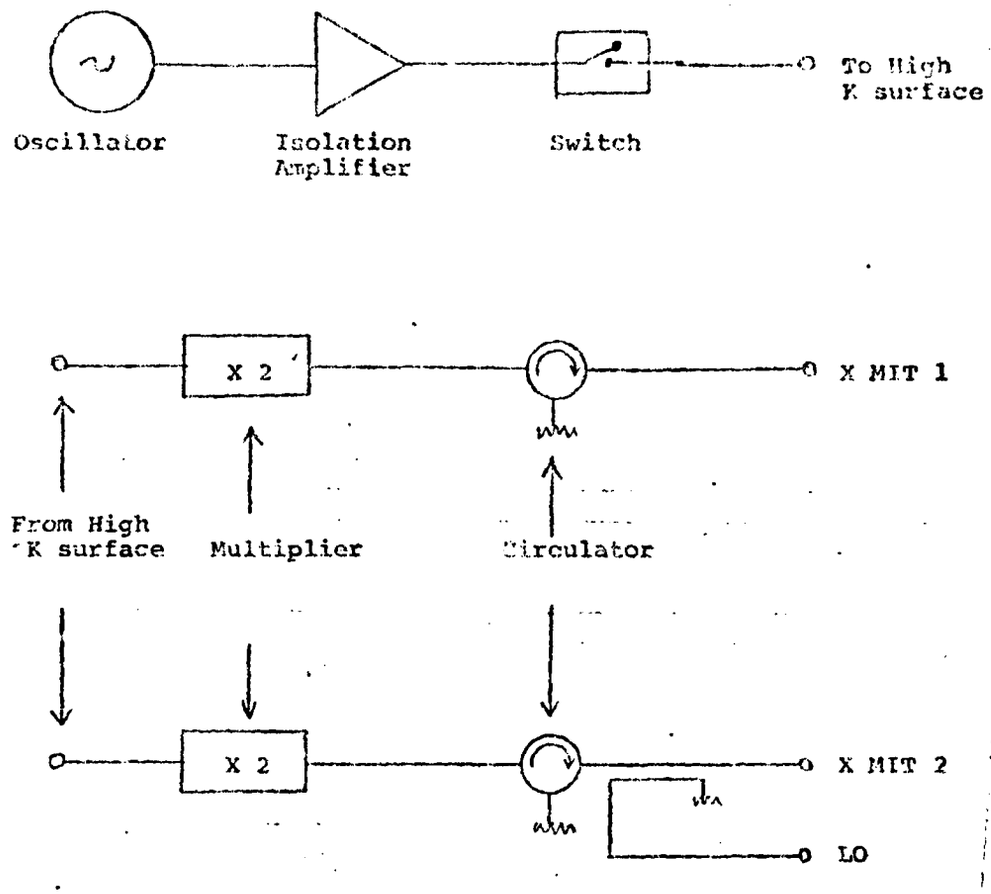

Figure 1 Block diagram of low K surface

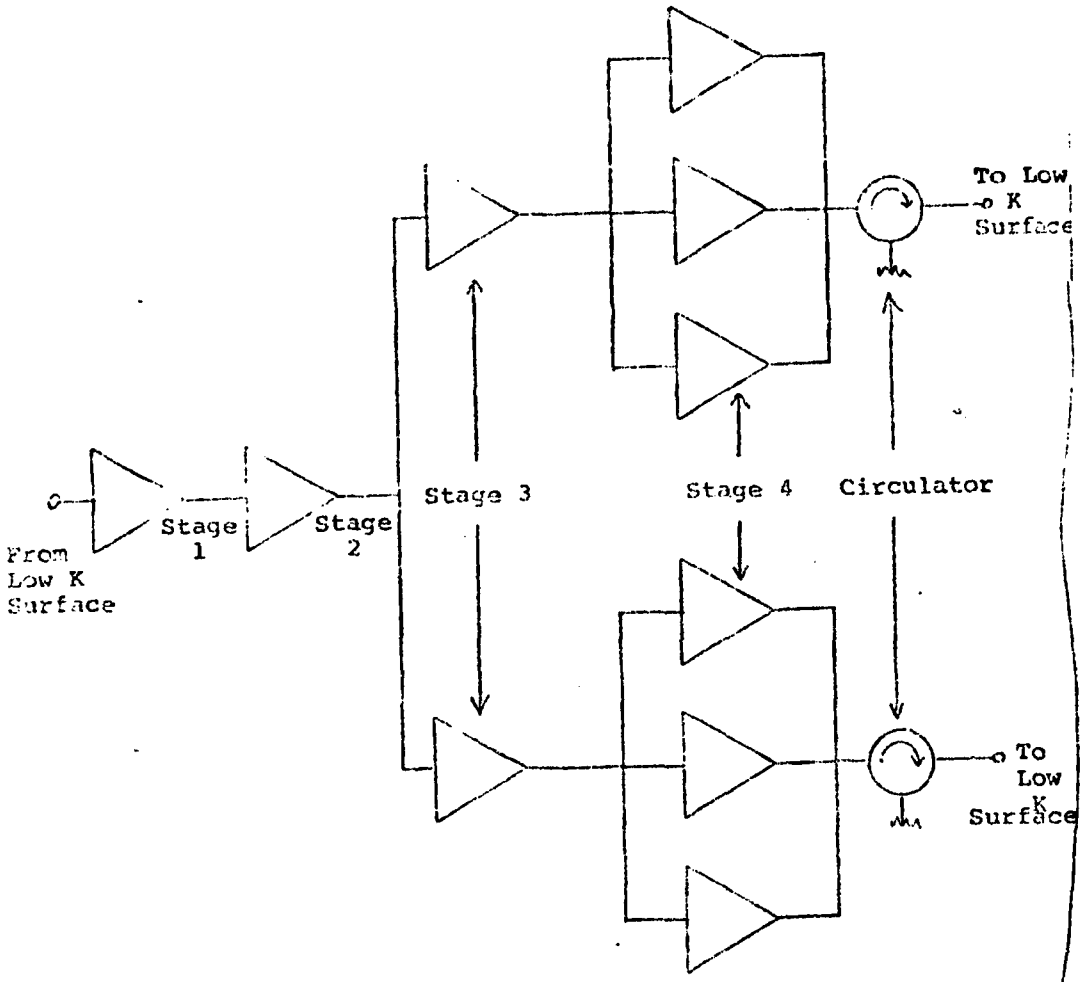

Figure 2 Block diagram of high K surface

TABLE I ELECTRICAL CHARACTERISTICS OF POWER TRANSISTOR

Pulse Width = 10 μsec, Duty = 1%, V_{cc} = +40v, Pin = 14w (PK)

S/N	BV_{EBO} @I_E = 20 mA (V)	BV_{CES} @I_C = 20 mA (V)	I_{CES} @V_{CE} = 35 V (mA)	h_{FE} @V_{CE} = 5V I_C = 500 mA	Po PEAK (w)	I_C PEAK (a)	M_C %
	ASSEMBLY 5692						
6	5.3	59	.21	46	86.4	5.85	36.9
10	5.3	59	2.2	42	74.5	5.05	36.9
13	5.4	58	1.4	50	82.1	6.3	32.6
14	5.3	59	1.1	47	77.4	5.35	36.2
15	5.3	59	3.0	49	80.2	5.75	34.9
18	5.4	59	.16	50	72.6	5.45	33.3
19	5.3	59	.60	42	84.0	5.85	37.8
	ASSEMBLY 5961						
11	5.3	60	2.0	46	78.8	5.55	35.5
17	5.3	61	.5	46	76.4	4.9	39.0
18	5.3	59	2.6	42	75.4	5.3	35.6

After the individual devices were tested, a three-way reactive splitter/combiner was designed and tuned for 195 watts of output power with an input level of 47 watts at room ambient. The power was down by 2.2 dB after non-operating cold soak at -40°C. Figure 3 is a plot of power out for different drive levels and it also shows the variation in power out across the temperature extremes at the 45 watt drive level.

2.3 Selection of Transistors for Remaining Amplifier Stages

The three drive stages employ MSC devices which were noteworthy for ruggedness, repeatability, and temperature stability. Driving each trio of PHI 8469A devices is an MSC 74034 which provides 45 watts minimum if driven with 8 watts. See figure 4 for drive characteristics. These two are driven by an MSC 81720-20 which is driven in turn by an MSC 1720-3. Representative drive levels of these devices are shown in figures 5 and 6, respectively.

All of the amplifier stages were designed on Epsilam 10 material (ϵ_r = 10.3) from 3M Company. A breadboard of all the amplifier stages on one piece of E-10 was fabricated and tested with an input power of 300 mw. Channel 1 had an output of 178 watts and channel 2 had an output of 182 watts.

Rise times on both were less than or equal to 20μsec. Table II shows the current requirements of individual stages and devices. Monitoring individual currents during the tuning phase enables optimum drive conditions to be met.

2.4 Oscillator Design

A silicon NPN bipolar transistor, Hewlett-Packard HXTR 5104, was chosen for the negative resistance oscillator. It was designed to operate at fo/2 at +24v bias on low dielectric constant (such as Rogers Duriod, (ϵ_r = 2.2). It was fabircated on a test block along with a circulator, the RF switch module and a driver circuit. Power generated and deliverable to the amplifier input was +26.6 dBM (457 mw) at ½ fo and +24 bias. For +25v, the frequency dropped 2 MHz and at +23v, it increased 2 MHz. Table III shows oscillator characteristics over temperature.

Subsequent tests on this circuit revealed an instability caused by the out-of-band characteristics of the circulator. It was replaced with an "isolation amplifier," a class A NPN transistor amplifier with 10 dB gain preceded by a 10dB pad.

2.5 Multiplier Design

The frequency doubler was designed on the low dielectric material around diodes manufactured by GHZ. They are part number 33131-47 with 5 chips in each for higher breakdown voltage and, thus, higher power capability. Capacitance was specified at 3 ± 10% pf.

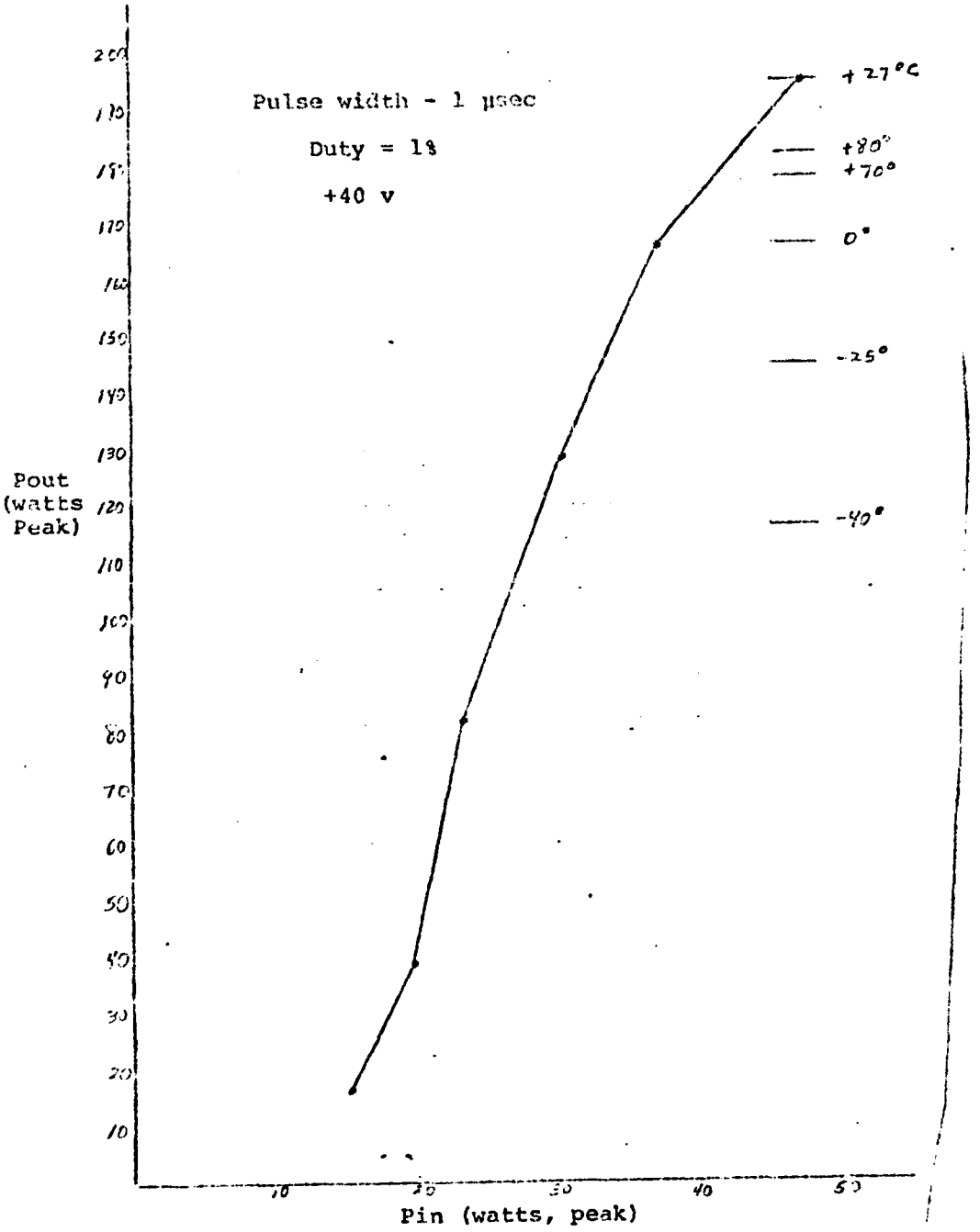

Figure 3 transistor trio power out versus power in

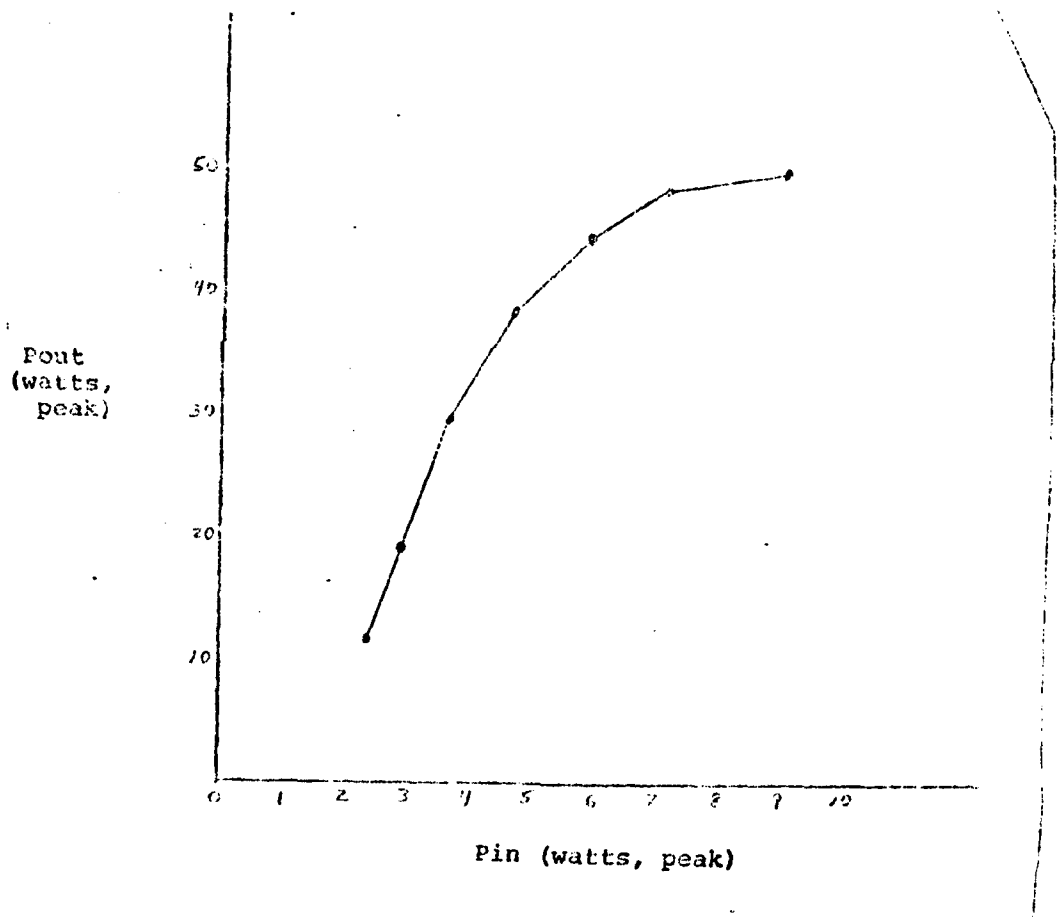

Figure 4 amplifier stage #3 power out versus power in

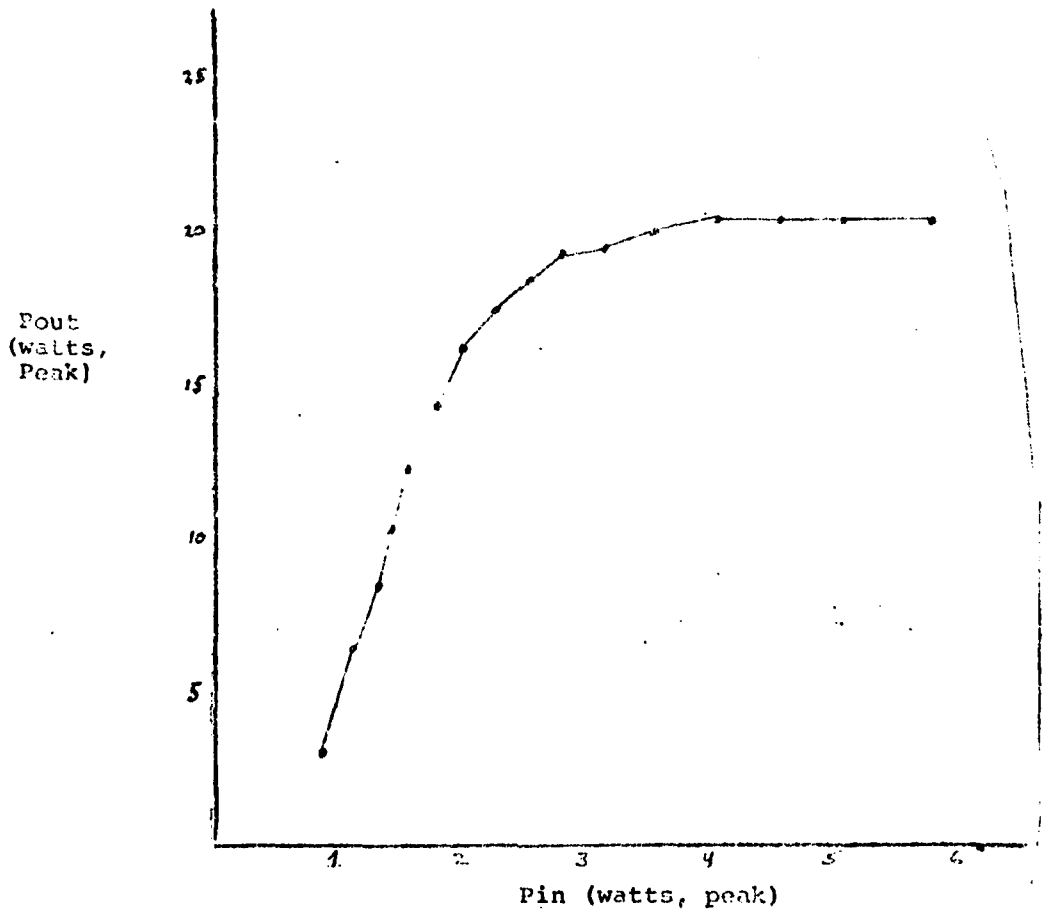

Figure 5 amplifier stage #2 power out versus power in

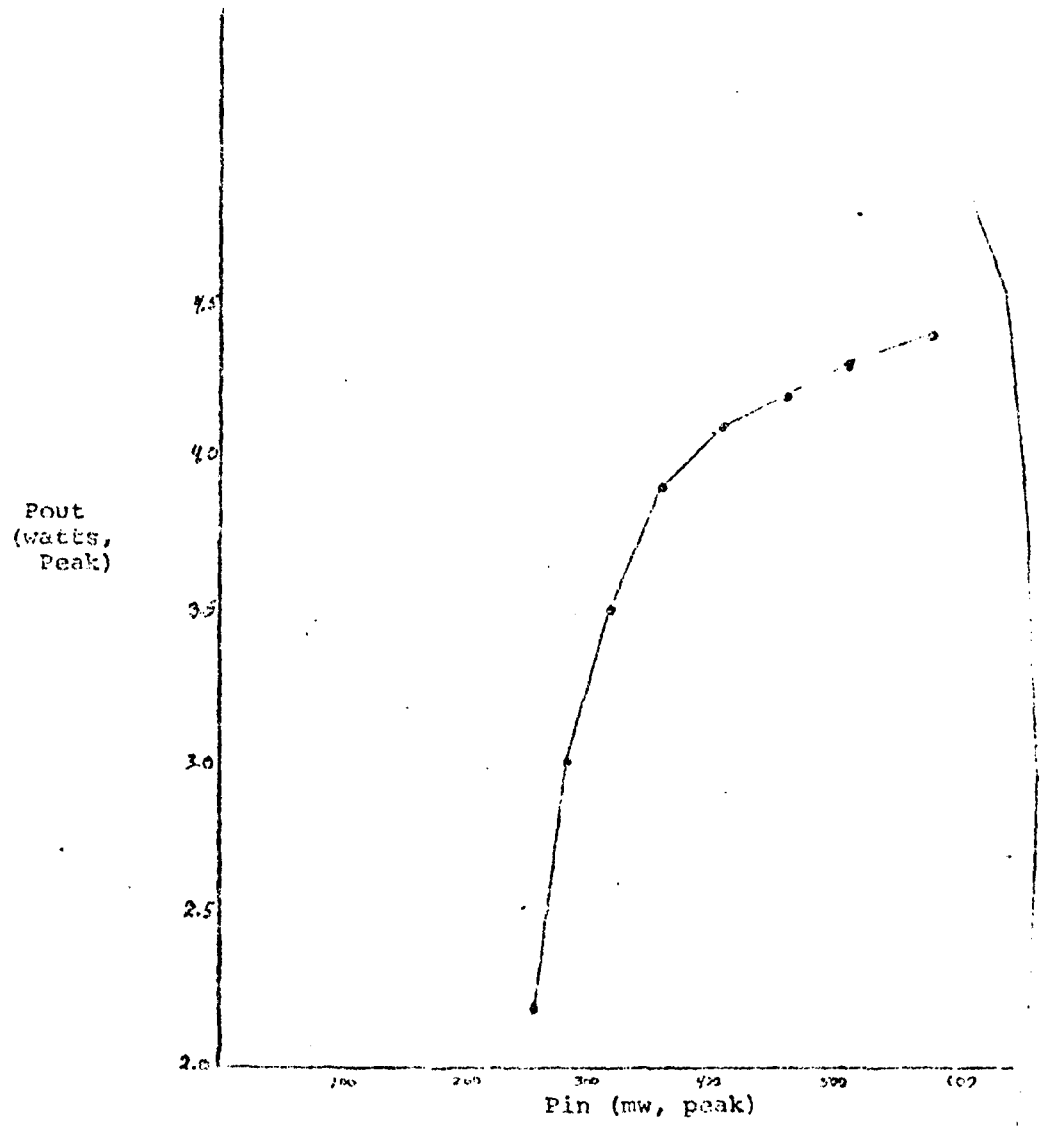

Figure 6 amplifier stage #1 power out versus power in

TABLE II BREADBOARD RESULTS OF AMPLIFIER STAGES
BUILT ON E-10

I_{24V}	I_{35V}	I_{40V}				P_{OUT} CH 1	P_{OUT} CH 2
		CHANNEL 1		CHANNEL 2			
		1 DEVICE	2 DEVICES	1 DEVICE	2 DEVICES		
19 ma	48 ma	49 ma	114 ma	48 ma	94 ma	178 W	182 W

TABLE III NEGATIVE RESISTANCE OSCILLATOR CHARACTERISTICS
VERSUS TEMPERATURE

P_{OUT} (dBM)	FREQ. (MHz)	TEMP	TIME	COMMENTS
26.8	Ref=R	+29°C	To	
26.7	R+13	-25°C	To + 20 min	After cold soak non-operating
26.6	R+9	Room Amb.		
26.4	R+3	+71°C	T1	
26.5	R-13	+71°C	T1 + 15 min	Unit running while warming
26.7	R-5	Room Amb.		

The results on the multiplier by itself showed P_{out} at fo was 91 watts for the 182 watts in at ½fo. Other characteristics are listed in Table IV. Checking the generated harmonic power levels there and considering the output circulator characteristics listed in Table V, one can determine that the required harmonic attenuation levels are met.

3.0 FINAL CONFIGURATION

3.1 Electrical

The TTL input signal provided is used to trigger a timing mechanism whereby the +24v bias to the oscillator is turned on for approximately 1500 nanoseconds for each pulse. The RF switch was timed to pass the signal for a duration of 100 nanoseconds during the latter half of the oscillator pulse. Pulsing the oscillator allows for overall higher efficiency as well as protecting the amplifiers against CW operation if a switch failure occurs.

Regulators were not included inside the units. Voltages of +5, -13.2, +24, +35, +40, and -50 were all brought in through standard EMI filters.

A loosely coupled line was added after the oscillator to provide a low level test signal at ½ fo and a backward-wave, quarter-wave coupler was added in Channel 2 as an LO output at fo.

3.2 Mechanical

Transition from one side of the circuit to the other was accomplished by carefully fabricating U-shaped pieces of 0.085" semi-rigid hardline coaxial cable and soldering each end to a small flange which could then be screwed to the base plate. The center pin of the coax is soldered to the 50 Ω Microstrip line for a reliable, low VSWR transition. (This method of interconnection also provides a test point whereby a piece of coax with a standard connector can be soldered to a flange and connected to the microstrip circuit.)

4.0 TEST RESULTS

4.1 Initial Test Results

Initial room temperature tests on serial number 1 indicated 81 watts at Channel 1 and 63 watts at Channel 2. After cold soak at -32°C, Channel 2 was dropped by 1.4 dB and Channel 1 had a deformed pulse shape making the relative average power reading meaningless.

On serial number 2, initial readings on power were 71 watts for Channel 1 and 50 watts on Channel 2. Rise times were 12 and 10 nanoseconds respectively, with fall times of 8 and 6 nanoseconds. Preliminary temperature tests resulted in pulse deformation hot and cold, indicating de-tuned amplifier stages probably caused by impedance changes in transistors.

TABLE IV FREQUENCY DOUBLER CHARACTERISTICS

P_{IN} (½ fo)	P_{OUT} (fo)	RETURN LOSS	HARMONICS			
			fo	½ fo	3/2 fo	2 fo
182 W	90 W	12 dB	REF=R	R-38 dB	R-38 dB	R-26 dB

TABLE V OUTPUT CIRCULATOR CHARACTERISTICS

S/N	FREQ	VSWR (dB)			INSERTION LOSS (dB)			ISOLATION (dB)		
	(GHz)	1	2	3	1-2	2-3	3-1	2-1	3-2	1-3
	fo	1.03	1.05	1.10	.35	.35	.35	>20	>20	>20
101	½fo	3.5				10				
	3/2fo	16				11				
	2fo	20				20				
	fo	1.05	1.16	1.06	.35	.35	.35	>20	>20	>20
102	½fo	3.5				10				
	3/2fo	15				12				
	2fo	26				23				

4.2 Final Test Results

Both units were temperature cycled non-operating from -45°C to +85°C for four days with two hours at each extreme in each cycle. Continuing attempts to tune for higher output power and better temperature performance were to no avail. Switching transistors and multiplier diodes were of no benefit and, if anything, the excessive circuit rework probably degraded the circuit.

Table VI and VII are the final data sheets for serial numbers 1 and 2, respectively. Note that in both units, the total noise power was below the noise of the amplifier used for the measurement per Westinghouse Acceptance Test Procedure MCP 605. This was true for all axes of vibration, as well as stationary.

5.0 CONCLUSIONS AND RECOMMENDATIONS

The work performed under this contract and the hardware produced clearly demonstrate the feasibility of manufacturing solid state transmitters at the 80 to 100 watt level at high S-band. As interest in such components increases, transistor developers strive to advance the state-of-the-art in terms of power and frequency in silicon bipolar devices. For example, MSC built a 100 watt sample 16 cell device in their standard ampac (.400" x .400") package in May of 1979. (At that time their standard 12 cell device was capable of about 65 watts at ½ fo.) Data on this device is shown in Tables VIII and IX.

Also, according to MSC, it is physically possible to fit an 18 cell device in the same size package. It is likewise reasonable to consider a larger package .400" x .500" which could accomodate 25 to 28 cells. Such a device would operate at +45v and deliver around 130 watts with reasonable gain. Impedance levels are lower as more cells are combined, but this should produce no major problem for single frequency operation. Development of such a device is estimated to be 9 to 12 months.

Rapidly advancing transistor technology and power combining techniques at S-band suggest that it may also be possible to generate and amplify the power at fo, eliminating the multiplier. MSC measured data in January of 1980 showing peak powers of 40watts at 3GHz, dropping off to about 25 watts at 3.5GHz. Both MSC and TRW are optimisitc in reaching 40 to 50 watts across the band from 3 to 3.5 GHz. It is reasonable to project that a device could be developed to be optimized for 40 or 50 watts single frequency in high S-band.

Whether additional work is done all at fo or at ½ fo with a frequency doubler, two distinct recommendations are clear:

(1) The substrate material should be all high K dielectric. This would reduce the size of the oscillator and multiplier and would necessitate an RF transition between faces only once.

(2) Power should be generated initially at a higher power level, thereby, eliminating two or more amplifier stages.

TABLE VI FINAL DATA, SERIAL NUMBER 1

SOLID STATE PULSED SOURCE

DATA SHEET

	XMIT 1			XMIT 2		
	+26°C	+71°C	[illegible]°C	+26°C	+71°C	[illegible]°C
Peak Power Out	63 w	58.5 w	63 w	70 w	59.3 w	67.5 w
Rise Time (10%—90%)	17 nsec	20 nsec	17 nsec	20 nsec	20 nsec	30 nsec
Fall Time (90%—10%)	14 nsec	17 nsec	10 nsec	12 nsec	14 nsec	17 nsec
Frequency	f_o -5 MHZ	f_o +5 MHZ	f_o -16 MHZ	f_o -5 MHZ	f_o +5 MHZ	f_o -16 MHZ
PULSE WIDTH AT 50% POINT	88 nsec	83 nsec	90 nsec	90 nsec	84 nsec	81 nsec

Total Noise Power (dBM)	-79	-79	-79	-79
	Static	X Axis	Y Axis	Z Axis

Tested By: L. M. Nelson

Date 12/11/79

S.N. 1

TABLE VII FINAL DATA, SERIAL NUMBER 2

SOLID STATE PULSED SOURCE

DATA SHEET

	XMIT 1			XMIT 2		
	+26°C	+50 +1 °C	-32°C	+26°C	+50 +1 °C	-32°C
Peak Power Out	70 w	41 w		70 w	50 w	
Rise Time (10%—90%)	20 nsec	33 nsec		22 nsec	30 nsec	
Fall Time (90%—10%)	10 nsec	8 nsec		12 nsec	13 nsec	
Frequency	f_o + 20 MHz	f_o + 27 MHz		f_o + 20 MHz	f_o + 27 MHz	
PULSE WIDTH AT 50% POINT	104 nsec	80 nsec		106 nsec	86 nsec	

Total Noise Power (dBM)	-76 Static	-76 X Axis	-76 Y Axis	-76 Z Axis

Tested By: Y. M. Nelson

Date 12/11/79

S.N. 2

TABLE VIII DRIVE CHARACTERISTICS OF MSC SAMPLE 16 CELL TRANSISTOR AT +40V, 5 μsec PULSE WIDTH, 10% DUTY

P_{IN} WATTS	P_{OUT} WATTS	I_{dc} amp (PK)
5	29	2.8
10	74	4.7
15	93.5	5.8
17.5	98	6.25
20	102	6.6

TABLE IX ELECTRICAL CHARACTERISTICS VERSUS VOLTAGE OF MSC SAMPLE 16 CELL TRANSISTOR AT 15 WATT INPUT POWER, 5 μsec PULSE WIDTH, 10% DUTY

V_{dc}	P_{OUT} WATTS	I_{dc} amp (PK)
35	80	5.2
38	88	5.4
40	92	5.6
42	94	5.85

APPENDIX A - DRAWING TABULATION

9RD 8003	Cover
9RD 8004	Carrier Detail, Low Dielectric Side
9RD 8005	End Rail, Output
9RD 8006	Transition Block
9RD 8007	Substrate Masks
9RD 8008	Side Rail
9RD 8009	Side Rail, Test Port
9RD 8010	End Rail
9RD 8011	Carrier Detail, High Dielectric Side
9RD 8012	Cover, Bottom
9RD 8013	Carrier Detail, Transitions
9RD 8014	Top Assembly, Low Dielectric Side
9RD 8015	Top Assembly, High Dielectric Side
9RD 8016	Carrier Detail, High Dielectric Side
9RD 8017	Carrier Detail
9RD 8018	Schematic
	Parts List